WHAT IS CLAIMED IS:

1. A carrier detection circuit (a) for creating a carrier detection level in accordance with an received signal, and (b) for detecting whether or not a carrier exists in the received signal in accordance with the carrier detection level, said carrier detection circuit comprising:

a detector for detecting groups of pulses, to be detected, having a carrier frequency; and

an integrator for carrying out integration of a time in which the groups of pulses are detected by said detector, and for outputting a resultant of the integration as the carrier detection level.

2. A carrier detection circuit as set forth in Claim 1, further comprising:

an offset circuit for adding an offset to the carrier detection level for comparison of the received signal with the carrier detection level.

3. A carrier detection circuit as set forth in Claim 1, further comprising:

a rapid charging circuit for temporarily supplying a large current into an output of said integrator, when the received signal has an amplitude level higher than

a predetermined level.

4. A carrier detection circuit as set forth in Claim 2, further comprising:

a rapid charging circuit for temporarily supplying a large current into an output terminal of said integrator, when the received signal has an amplitude level higher than a predetermined level.

5. The carrier detection circuit as set forth in Claim 3, in which said rapid charging circuit is a diode.

6. The carrier detection circuit as set forth in Claim 4, in which said rapid charging circuit is a diode.

7. A carrier detection circuit as set forth in Claim 1, further comprising:

a buffer, provided in a position for monitoring a voltage in an integration capacitor of said integrator, wherein a ratio of (a) an input bias current of said buffer, which is a discharging current out of said capacitor, to (b) a charging current into said capacitor from said integrator is set to be constant.

8. A carrier detection circuit as set forth in Claim 2, further comprising:

a buffer, provided in a position for monitoring a voltage in an integration capacitor of said integrator, wherein a ratio of (a) an input bias current of said buffer, which is a discharging current out of said capacitor, to (b) a charging current into said capacitor from said integrator is set to be constant.

9. A carrier detection circuit as set forth in Claim 3, further comprising:

a buffer, provided in a position for monitoring a voltage in an integration capacitor of said integrator, wherein a ratio of (a) an input bias current of said buffer, which is a discharging current out of said capacitor, to (b) a charging current into said capacitor from said integrator is set to be constant.

10. A carrier detection circuit as set forth in Claim 4, further comprising:

a buffer, provided in a position for monitoring a voltage in an integration capacitor of said integrator, wherein a ratio of (a) an input bias current of said buffer, which is a discharging current out of said capacitor, to (b) a charging current into said

capacitor from said integrator is set to be constant.

11. The carrier detection circuit as set forth in Claim 7, wherein the charging current from said integrator into said integration capacitor is a base current of a vertical PNP transistor, while the input bias current of said buffer is a base current of an NPN transistor.

12. The carrier detection circuit as set forth in Claim 8, wherein the charging current from said integrator into said integration capacitor is a base current of a vertical PNP transistor, while the input bias current of said buffer is a base current of an NPN transistor.

13. The carrier detection circuit as set forth in Claim 9, wherein the charging current from said integrator into said integration capacitor is a base current of a vertical PNP transistor, while the input bias current of said buffer is a base current of an NPN transistor.

14. The carrier detection circuit as set forth in Claim 10, wherein the charging current from said

integrator into said integration capacitor is a base current of a vertical PNP transistor, while the input bias current of said buffer is a base current of an NPN transistor.

15. A carrier detection circuit as set forth in Claim 1, further comprising:

a current mirror circuit for compensating a parasite light current, in association with a PNP transistor for creating feeble currents of charging and discharging an integration capacitor of said integrator.

16. A carrier detection circuit as set forth in Claim 2, further comprising:

a current mirror circuit for compensating a parasite light current, in association with a PNP transistor for creating feeble currents of charging and discharging an integration capacitor of said integrator.

17. A carrier detection circuit as set forth in Claim 3, further comprising:

a current mirror circuit for compensating a parasite light current, in association with a PNP

transistor for creating feeble currents of charging and discharging an integration capacitor of said integrator.

18. A carrier detection circuit as set forth in Claim 4, further comprising:

a current mirror circuit for compensating a parasite light current, in association with a PNP transistor for creating feeble currents of charging and discharging an integration capacitor of said integrator.

19. A carrier detection circuit as set forth in Claim 7, further comprising:

a current mirror circuit for compensating a parasite light current, in association with a PNP transistor for creating feeble currents of charging and discharging an integration capacitor of said integrator.

20. A carrier detection circuit as set forth in Claim 8, further comprising:

a current mirror circuit for compensating a parasite light current, in association with a PNP transistor for creating feeble currents of charging and

discharging an integration capacitor of said integrator.

21. A carrier detection circuit as set forth in Claim 9, further comprising:

a current mirror circuit for compensating a parasite light current, in association with a PNP transistor for creating feeble currents of charging and discharging an integration capacitor of said integrator.

22. A carrier detection circuit as set forth in Claim 10, further comprising:

a current mirror circuit for compensating a parasite light current, in association with a PNP transistor for creating feeble currents of charging and discharging an integration capacitor of said integrator.

23. The carrier detection circuit as set forth in Claim 15, wherein the current mirror circuit for compensating the parasite light current has an expitaxial island having an area larger than an area of an expitaxial island of said PNP transistor to be compensated.

24. The carrier detection circuit as set forth in Claim 16, wherein the current mirror circuit for compensating the parasite light current has an expitaxial island having an area larger than an area of an expitaxial island of said PNP transistor to be compensated.

25. The carrier detection circuit as set forth in Claim 17, wherein the current mirror circuit for compensating the parasite light current has an expitaxial island having an area larger than an area of an expitaxial island of said PNP transistor to be compensated.

26. The carrier detection circuit as set forth in Claim 18, wherein the current mirror circuit for compensating the parasite light current has an expitaxial island having an area larger than an area of an expitaxial island of said PNP transistor to be compensated.

27. The carrier detection circuit as set forth in Claim 19, wherein the current mirror circuit for compensating the parasite light current has an expitaxial island having an area larger than an area of

an expitaxial island of said PNP transistor to be compensated.

28. The carrier detection circuit as set forth in Claim 20, wherein the current mirror circuit for compensating the parasite light current has an expitaxial island having an area larger than an area of an expitaxial island of said PNP transistor to be compensated.

29. The carrier detection circuit as set forth in Claim 21, wherein the current mirror circuit for compensating the parasite light current has an expitaxial island having an area larger than an area of an expitaxial island of said PNP transistor to be compensated.

30. The carrier detection circuit as set forth in Claim 22, wherein the current mirror circuit for compensating the parasite light current has an expitaxial island having an area larger than an area of an expitaxial island of said PNP transistor to be compensated.

31. A carrier detection circuit for detecting

whether or not a carrier exists in an received signal, in accordance with a carrier detection level, comprising:

a detector for detecting groups of pulses having a carrier frequency in an received signal, in accordance with the carrier detection level; and

an integrator for carrying out an integration of an output signal of said detector, and for outputting a resultant of the integration as the carrier detection level.

32. The carrier detection circuit as set forth in Claim 31, wherein said detector includes:

an amplifier for amplifying a difference between the received signal and the carrier detection level;

a rectifier for rectifying an output voltage of said amplifier;

a capacitor for being charged with the output voltage of said amplifier via said rectifier, a voltage across said capacitor being outputted as the output signal; and

a constant current source, connected with said capacitor in parallel, for discharging the capacitor via a constant current.

33. The carrier detection circuit as set forth in Claim 32, wherein a ratio of the charging current to the discharging current of said capacitor is constant.

34. A carrier detection circuit as set forth in Claim 31, further comprising:

an offset circuit for adding an offset voltage into the received signal or the carrier detection level.

35. The carrier detection circuit as set forth in Claim 34, wherein said offset circuit includes:

a pair of first and second transistors whose bases receive differential received signals, respectively;

first and second load resistors, connected with emitters of said first and second transistors, respectively;

a first constant current source for supplying currents to said first and second transistors via said first and second load resistors;

third and fourth transistors, connected with said first and second transistors, for configuring a current mirror circuit, said third and fourth transistors occupying areas , which are identical to each other, of said current mirror circuit, respectively;

a fifth transistor whose base receives a voltage between collectors of said first and third transistors; and

a second constant current source for supplying a constant current to an emitter of said fifth transistor.

36. A carrier detection circuit as set forth in Claim 31, further comprising:

a rapid charging circuit for rapidly charging said capacitor, when the received signal exceeds the carrier detection level.

37. A carrier detection circuit as set forth in Claim 34, further comprising:

a rapid charging circuit for rapidly charging said capacitor, when the received signal exceeds a predetermined level.

38. The carrier detection circuit as set forth in Claim 32, wherein the received signal and the carrier detection level are supplied into said detection circuit via first and second buffers, respectively.

39. A carrier detection circuit for generating a

carrier detection level in accordance with an received signal so as to detect, in accordance with the carrier detection level, whether or not a carrier exists in the received signal, said carrier detection circuit, comprising:

a detector for detecting pulses, to be detected, having a carrier frequency;

an integrator for performing integration of a time in which an output of said detector is higher than a predetermined reference integral value, so as to detect groups of the pulses having the carrier frequency, and for outputting a resultant of the integration as the carrier detection level; and

a level change-over circuit for increasing the output of said detector relative to the reference integral value, during a time in which a carrier exists.

40. The carrier detection circuit as set forth in Claim 39, wherein said level change-over circuit limits the output of said detector at a constant voltage that is slightly higher than the reference integral value, so as to increase the output of said detector relative to the reference integral value, during the time carrier exists.

41. The carrier detection circuit as set forth in Claim 39, wherein said level change-over circuit reduces a discharging current of a capacitor in an output stage of said detector, so as to increase the output of said detector relative to the reference integral value, during the time in which the carrier exists.

42. The carrier detection circuit as set forth in Claim 39, wherein said level change-over circuit increases an input offset voltage of an received signal to be supplied into said detector, so as to increase the output of said detector relative to the reference integral value, during the time in which the carrier exists.

43. The carrier detection circuit as set forth in Claim 39, wherein said level change-over circuit lowers the reference integral value of said integrator, so as to increase the output of said detector relative to the reference integral value, during the time in which the carrier exists.

44. An infrared ray remote control receiver, incorporated with a carrier detection circuit for

creating a carrier detection level in accordance with an received signal, so as to detect, in accordance with the carrier detection level, whether or not the carrier exists in the received signal, said carrier detection circuit, including:

a detector for detecting pulses, to be detected, having a carrier frequency;

an integrator for detecting groups of the pulses having the carrier frequency by performing integration of a time in which an output of said detector is higher than a predetermined reference integral value, and for outputting a resultant of the integration as the carrier detection level; and

a level change-over circuit for increasing the output of said detector relative to the reference integral value, during a time in which a carrier exists.

45. The carrier detection circuit as set forth in Claim 44, wherein said level change-over circuit limits the output of said detector at a constant voltage that is slightly higher than the reference integral value, so as to increase the output of said detector relative to the reference integral value, during the time carrier exists.

46. The carrier detection circuit as set forth in Claim 44, wherein said level change-over circuit reduces a discharging current of a capacitor in an output stage of said detector, so as to increase the output of said detector relative to the reference integral value, during the time in which the carrier exists.

47. The carrier detection circuit as set forth in Claim 44, wherein said level change-over circuit increases an input offset voltage of an received signal for said detector, so as to increase the output of said detector relative to the reference integral value, during the time in which the carrier exists.

48. The carrier detection circuit as set forth in Claim 44, wherein said level change-over circuit lowers the reference integral value of said integrator, so as to increase the output of said detector relative to the reference integral value, during the time in which the carrier exists.

49. An infrared ray remote control receiver (a) for inputting an received signal, which has been obtained by receiving an infrared ray signal, into a

band pass filter via an amplifier, so as to detect the carrier frequency components, to be detected, in the received signal, (b) for subsequently detecting pulses having the carrier frequency by using carrier detection circuit, so as to perform integration of a time in which a resultant of the detection is higher than a predetermined reference integral value, thereby detecting groups of the pulses having the carrier frequency, while detecting whether or not a carrier exists in the received signal, in accordance with an output of the integration as a carrier detection level, said infrared ray remote control receiver, comprising:

a gain change-over circuit for lowering at least either of a gain of said amplifier or a gain of band pass filter, during a time in which the carrier is detected.

50. The infrared ray remote control receiver as set forth in Claim 49, wherein said gain change-over circuit is given a time constant while said gain change-over circuit is lowering the gain.